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APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/042,408	(	01/08/2002	Naoki Fukutomi	7426-082	9036	
20457	7590	05/13/2004		EXAMINER		
		RY, STOUT & KR	BEREZNY, NEMA O			
1300 NORTH SEVENTEENTH-STREET - SUITE 1800			ART UNIT	PAPER NUMBER		
ARLINGTO		22209-9889		2813		

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

e		<i>j</i> :	
	Application No.	Applicant(s)	
	10/042,408	FUKUTOMI ET AL.	
Office Action Summary	Examiner	Art Unit	
	Nema O Berezny	2813	
The MAILING DATE of this communication Period for Reply	appears on the cover sheet w	ith the correspondence address	
A SHORTENED STATUTORY PERIOD FOR RETHE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by sany reply received by the Office later than three months after the rearned patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no event, however, may a n. a reply within the statutory minimum of thi eriod will apply and will expire SIX (6) MOI statute, cause the application to become A	reply be timely filed  ty (30) days will be considered timely.  THS from the mailing date of this communication  BANDONED (35 U.S.C. § 133).	- · ion.
Status			
1)⊠ Responsive to communication(s) filed on 2 2a)⊠ This action is <b>FINAL</b> . 2b)□ 3)□ Since this application is in condition for all closed in accordance with the practice uncondition.	This action is non-final. owance except for formal mat		is
Disposition of Claims			
4)	is/are withdrawn from consid	eration.	
Application Papers			
9) The specification is objected to by the Example 10) The drawing(s) filed on 28 August 2002 is Applicant may not request that any objection to Replacement drawing sheet(s) including the control of the oath or declaration is objected to by the	are: a)⊠ accepted or b)□ o o the drawing(s) be held in abeya orrection is required if the drawing	nce. See 37 CFR 1.85(a). g(s) is objected to. See 37 CFR 1.121	
Priority under 35 U.S.C. § 119			
12) ☐ Acknowledgment is made of a claim for for a) ☐ All b) ☐ Some * c) ☐ None of:  1. ☐ Certified copies of the priority docur 2. ☐ Certified copies of the priority docur 3. ☐ Copies of the certified copies of the application from the International But * See the attached detailed Office action for a	ments have been received. ments have been received in a priority documents have been ureau (PCT Rule 17.2(a)).	Application No  n received in this National Stage	
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/S Paper No(s)/Mail Date	Paper No	Summary (PTO-413) (s)/Mail Date Informal Patent Application (PTO-152) 	

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#### **DETAILED ACTION**

## Specification

Cancellation of claims 22-23 and 26 in paper filed 4-26-04 is acknowledged.

#### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

Claims 25, 31-34, and 36-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Marrs et al. (5,355,283). Marrs discloses a substrate for mounting semiconductor devices thereon having an insulating supporting member (Fig.2 el.202; col.7 lines 26-30) and plural sets of wirings (el.205), and further comprising: a semiconductor device mounting region (el.202) and a resin-sealing semiconductor package region (el.203) outside of said semiconductor device mounting region, wherein said plural sets of wirings comprise a predetermined wiring pattern including wirebonding terminals (el.205) and external connection terminals (el.208), wherein said wire bonding terminals are provided in said semiconductor package region and said external connection terminals are provided in said semiconductor device mounting region

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(Fig.2), wherein said substrate includes a plurality of said semiconductor device mounting regions (col.4 line 66 – col.5 line 2), and wherein said plurality of said semiconductor device mounting regions respectively have blocks of said wirings, each having a same pattern (Fig.2) [claim 32]. Marrs also discloses wherein said external connecting terminals are exposed on a surface of said insulating supporting member, on opposite side of which said semiconductor device is mounted (Fig.2), and are arranged in a grid pattern at positions corresponding to said semiconductor device mounting region and said semiconductor packaging region (col.1 lines 25-35, 48-51) [claim 25]; wherein said wirings form a predetermined wiring pattern including a wire bonding terminal (el.205) and an external connection terminal (el.208); and said external connection terminal is provided only inside of said wire bonding terminal (Fig.2) Iclaim 331; comprising a plurality of said wiring patterns comprised of a plurality of said wirings arranged in rows and columns (col.1 lines 25-35, 48-51) [claim 34]; and wherein said external connection terminal is one of a plurality of external connection terminals, exposed on a surface of said insulating supporting member, on an opposite side to which said semiconductor device is mounted, and said external connection terminals are arranged in a grid patterns at positions corresponding to a semiconductor device mounting region and a semiconductor package region of said substrate (col.1 lines 25-35, 48-51) [claim 36]. Marrs also discloses the semiconductor package (el.200) produced by a method comprising the steps of: mounting a semiconductor device on each of said plural semiconductor devices mounting regions of the substrate for mounting semiconductor device thereon according to claim 32 or 33 by employing a

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die bonding material; electrically connecting said semiconductor device with said wire-bonding terminal by wire-bonding; sealing said semiconductor package region including said plural semiconductor devices with a sealing resin connected in one-piece; forming solder bumps on said external connection terminals; and cutting said substrate for mounting semiconductor devices thereon and said sealing resin in one operation to be separated into the individual semiconductor package [claims 31, 37].

#### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs as applied to claims 32-33 above, and further in view of Katsuhiko (JP 59208756). Marrs discloses a gold plate layer (col.3 lines 60-63) on the surface of said wire-bonding terminal. However, Marrs does not disclose a nickel layer on said terminal. Katsuhiko discloses wherein said wire-bonding terminal is formed in said semiconductor packaging region, and said wire-bonding terminals comprise a nickel and gold plate layer on its surface (Constitution). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the nickel plated wiring structures of Katsuhiko with the substrate of Marrs, in order to protect the terminal and facilitate wire bonding.

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### Response to Arguments

Applicant's arguments with respect to claims 22-26 and 31 have been considered but are most in view of the new ground(s) of rejection.

#### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 8:30-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Craig a. Thompson PRIMARY EXAMINER